Docket No. 60173 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	C. Huang	CONF. NO.:	7288
U.S. SERIAL NO:	10/696,198	EXAMINER:	H. Trinh
FILED:	October 28, 2003	GROUP:	2814
FOR:	MULTI-CHIP PACKAGE DEVICE WITH HEAT SINK AND FABRICATION METHOD THEREOF		

please do not enter
/(Vikki) Hoa B. Trinh/

Commissioner for Patents
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Sir/Madam:

AMENDMENT

Applicant is in receipt of the Office Action dated May 30, 2007 of the above-referenced application. Please amend the application as follows:

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A multi-chip package device with a heat sink, comprising:

a chip carrier;

at least one first chip mounted on and electrically connected to a surface of the chip carrier;

at least one semiconductor package mounted on and electrically connected to the surface of the chip carrier, wherein the semiconductor package is slightly thicker than the first chip; and

the heat sink mounted via an adhesion layer on a surface of the first chip and a surface of the semiconductor package that are opposite to surfaces of the first chip and the semiconductor package mounted on the chip carrier, wherein a portion of the heat sink attached to the first chip is made thicker than another portion of the heat sink mounted on the semiconductor package, and at least one hollow part extending through the heat sink is formed at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink through the at least one hollow part that remains hollow, wherein the size of the hollow part is adjusted depending on the thickness of the heat sink to effectively release the thermal stresses from the heat sink.

Claim 2 (original): The multi-chip package device of claim 1, wherein the semiconductor package is a flip-chip ball grid array package.

Claim 3 (original): The multi-chip package device of claim 1, wherein the first chip is a graphic chip.

Claim 4 (original): The multi-chip package device of claim 1, wherein the first chip is a graphic processing unit.

Claim 5 (original): The multi-chip package device of claim 1, wherein the semiconductor package is a Random Access Memory (RAM) unit.

Claim 6 (original): The multi-chip package device of claim 1, wherein the first chip is mounted at the center of the chip carrier, and the semiconductor package is mounted at a position on the chip carrier corresponding to a corner of the heat sink.

Claim 7 (original): The multi-chip package device of claim 1, wherein at least one pair of the semiconductor packages are mounted on the chip carrier, and the hollow part of the heat sink is located between the semiconductor packages.

Claim 8 (original): The multi-chip package device of claim 1, wherein at least one symmetrical pair of the hollow parts are formed through the heat sink.

Claims 9-18 (canceled)

REMARKS

Claims 1-8 are pending in the application. Claim 1 has been amended by the present amendment. The amendment is fully supported by the application as originally filed (see, e.g., specification at page 10, lines 4-16; and page 11, lines 21-23).

As amended, independent claim 1 recites a multi-chip package device in which a heat sink includes at least one hollow part adjusted in size depending on the thickness of the heat sink to effectively release thermal stresses from the heat sink (see specification at page 10, lines 4-16; and page 11, lines 21-23).

For example, as shown in FIG. 4b of the application, the heat sink 34 includes hollow parts 34a that are sized to "effectively release thermal stresses from the heat sink 34 where the first chip 32 is attached" (see specification at page 10, lines 6-12). In other words, the size of the hollow parts 34a is "flexibly adjusted" to achieve effective stress release (see specification at page 11, lines 21-23).

According to the Applicant's claimed invention, thermal stresses generated by the heat sink can be released via the hollow parts, which can eliminate delamination of the heat sink from the chip or semiconductor package, chip cracking, structural warpage, and deterioration of electrical connections (see, e.g., specification at page 10, line 17 to page 11, line 4).

Claims 1-4 and 6-8 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent Application Publication US 2004/0099945 to Ku (hereinafter "Ku"). Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Ku in view of U.S. Patent 5,598,033 to Behlen et al. These rejections are respectfully traversed.

The Ku reference does not teach or suggest a multi-chip package device in which a heat sink includes at least one hollow part adjusted in size depending on the thickness of the heat sink to effectively release thermal stresses from the heat sink, as recited in independent claim 1.

On page 3 of the Office Action of 05/30/2007, an aperture 504 of a thermal bridge 50 was cited as allegedly corresponding to the Applicant's claimed "at least one hollow part."

In Ku, the aperture 504 is used "to accommodate the chips for saving material and facilitating the flow path design in forming the encapsulant 20 on the substrate 10" (see paragraph 0050 of Ku).

However, there is no teaching or suggestion in Ku that the aperture 504 can somehow be adjusted in size to "effectively release the thermal stresses from the heat sink" *as claimed.* In Ku, the aperture 504 is provided merely to save material and facilitate flow design.

For at least the reasons discussed above, the Ku reference does not anticipate or otherwise render obvious the Applicant's claimed invention. Therefore, independent claim 1 and dependent claims 2-8 are patentable over Ku.

Regarding the rejection of claim 6 over Ku, on page 4 of the Office Action of 05/30/2007, it was alleged that the chips 30 or 31 of Ku are mounted at the "center" of the substrate 10 in Ku. However, as shown in FIG. 4 of Ku, the chips 30 and 31 clearly are not mounted at the center of the substrate 10.

Moreover, reference number 10 of Ku was cited as allegedly corresponding to both a "semiconductor package" and a "chip carrier." However, claim 6 requires that the semiconductor package is mounted at a position on the chip carrier corresponding to a corner of the heat sink. To satisfy the claimed mounting arrangement, the substrate 10 of Ku cannot be considered both a semiconductor package and a chip carrier, i.e., the substrate 10 of Ku is not mounted on itself. Further, the encapsulant 20 of Ku cannot be considered a "semiconductor package" because it merely covers and seals the chips (see, e.g., paragraph 0048 of Ku), and thus does not correspond to a "semiconductor package."

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

/Steven M. Jensen/

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